**2024 NDIA MICHIGAN CHAPTER**
**GROUND VEHICLE SYSTEMS ENGINEERING**
**AND TECHNOLOGY SYMPOSIUM**
**POWER & MOBILITY TECHNICAL SESSION**
**AUGUST 13-15, 2024 - NOVI, MICHIGAN**

# A Compact, 100V, 360A Full-Bridge GaN Power Module with Integrated Gate Driver Board

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## ABSTRACT

*In this paper, the design analysis and development of a 100V, 360A Gallium Nitride (GaN) module is provided. This module has a full-bridge (FB) configuration with four 100V, 90A GaN bare die in parallel per switching position. The design challenges for current distribution on paralleled GaN bare die in a full-bridge module with a small footprint is elaborated with two module designs. To optimize the layout and perform parasitic extraction, Q3D and SIMPLORER tools in ANSYS simulation are utilized.*

*The selected power module design is fabricated. To validate the design and characterization, static and dynamic tests have been performed on this module. The gate driver design details, and power module loss evaluation techniques are discussed. Moreover, the voltage overshoot and resonance are studied and tested using double pulse test (DPT) setup.*

**Keywords:** Full-Bridge (FB) configuration, Gallium Nitride (GaN) MOSFETs, power overlay (POL), gate driver, double-pulse test (DPT).

## 1. INTRODUCTION

The goal of this paper is to discuss the design and fabrication of a compact, highly integrated 100V, 360A full-bridge GaN power module that can operate in a high-temperature environment. In the realm of low-voltage, high-current power converters, such GaN-based power modules emerge as a promising technology especially for certain military industry applications.

In appropriate voltage ranges, GaN devices are a great candidate for reducing switching losses and increasing system power density in high-temperature environments thanks to their low switching losses and near-zero reverse recovery [1]. Because of smaller gate

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charge requirement, GaN has higher switching speed in comparison with its silicon (Si) and silicon carbide (SiC) counterparts, enabling smaller passive components with higher switching frequency. The high di/dt, however, can easily increase the voltage overshoot with such a fast-switching condition and reduce current capability of a power module if combined with a high module loop inductance [2].

Several power module packaging methods are studied to reduce the power module loop inductance. One of the methods is using inductance minimization with multi-layer Printed Circuit Boards (PCB) or Insulated Metal Substrate (IMS) boards [3], [4]. While multi-layer boards are ideal solution for reducing the loop inductance through mutual inductance cancellation, the limited thermal capability on both IMS and PCBs limits the use of the overall GaN power module package to its full potential. The thermal conductivities of FR4 PCBs and IMS boards are ~0.3 W/mK and 3~7 W/mK respectively, while aluminum nitride (AlN) Direct Bond Copper (DBC) have thermal conductivity of 180~230 W/mK [4].

Another technique to minimize the switching loop inductance to the lowest level is using embedded high-frequency capacitors inside the power module. The capacitors embedded as close as possible to the switching positions across the positive and negative buses are called X-capacitors. This method allows the use of DBCs within the module package which provides a much higher thermal conductivity and hence is preferred for high-temperature applications. While X-capacitors can reduce the switching loop inductance significantly by eliminating the busbar inductance in the switching loop, special care should be taken for choosing correct X-capacitor temperature range and number of X-capacitors in parallel in a high-temperature environment.

## 2. GAN AND VOLTAGE OVERSHOOT

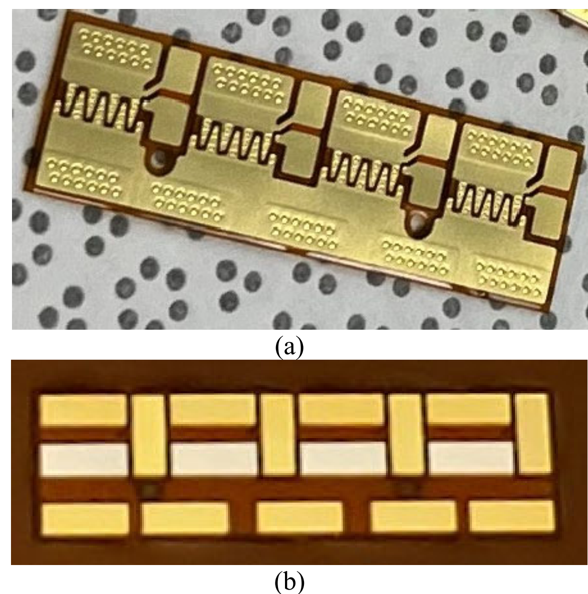
Because of very fast turn-on and turn-off of GaN devices, controlling the voltage overshoot can be challenging. LTSpice simulations show that without integrated X-capacitors the voltage overshoot on the bare die is so high that the module cannot meet the current requirements of the designed module.

Integrating the X-capacitors within the module, however, requires correct understanding of the capacitor/terminal/ half-bridge positions. Section 3 provides information on the details of module design and its effects on overall module performance.

## 3. MODULE DESIGN ANALYSES

### 3.1. Module Design: Current Distribution

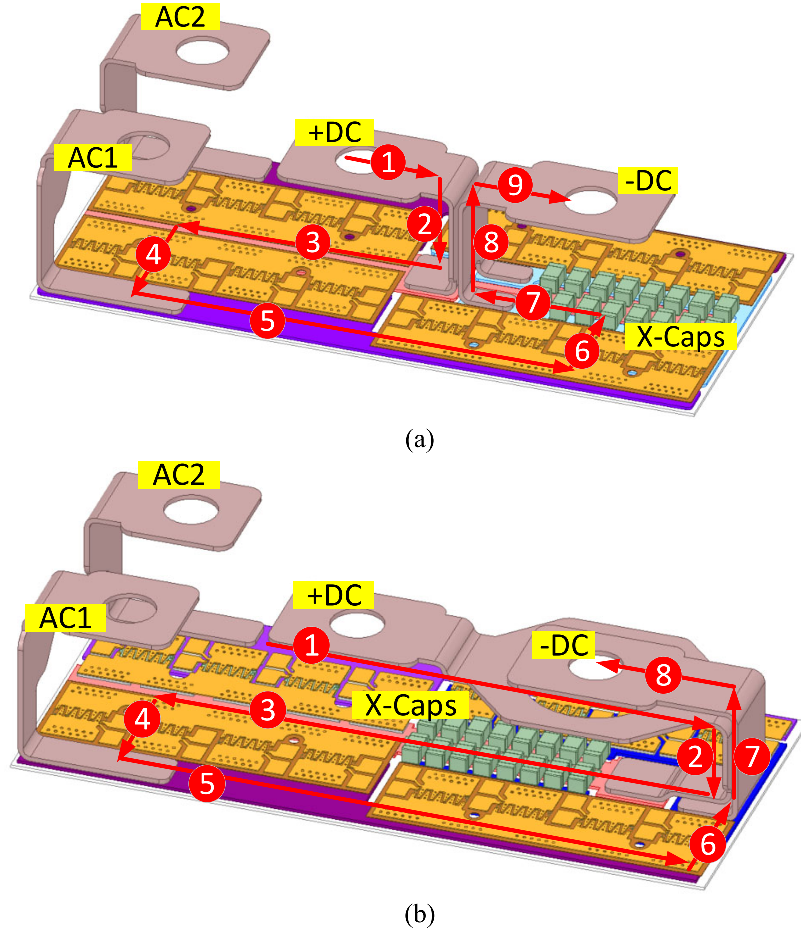
The proposed full-bridge (FB) GaN power module has a footprint of 36×82 mm$^2$; and is highly integrated considering its current capability of 360A. The module structure uses power-overlay (POL) technology which allows eliminating the wire-bonding and paralleling bare die in a much smaller footprint. Figure 1 shows the GaN POL designed for the proposed power module.



(a)

(b)

**Figure 1:** Power-Overlay (POL), a) top side, b) bottom side.




(a)

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**Figure 2:** 100V, 360A full-bridge GaN power module, a) module design A, b) module design B.

In this paper, two module designs were initially proposed. Both modules had sixteen integrated X-capacitors, eight capacitors in parallel with each half-bridge. Figure 2 shows the first power module design with the positive and negative DC busbars positioned at the center of the power module half-bridges.

Using ANSYS Q3D, the loop inductance between the positive and negative busbars is close to 3nH in module design A. However, having the X-capacitors closer to the bottom switching position and especially before the start point of the current circulation, i.e., DC busbars reduces the effectiveness of X-capacitor bank in this design. Figure 2(b) shows the second module design. The busbar location with respect to the X-capacitors and the switches has changed in a way that the capacitors are closer to both top and bottom switching positions and they are located after the DC busbars in the loop.

The detailed current circulation paths are provided with numbers for both module designs in Figures 2(a) and (b). In module design A, the current starts circulating from +DC busbar, *current paths 1 and 2*, through the top switching position, *current paths 3 and 4*, and then back into the bottom switching position, *5 and 6*, and eventually to the X-capacitors, *current path 7*, back to -DC busbar, *paths 8 and 9*.

In module design B, the current starts circulating from +DC busbar, *paths 1 and 2*, distributes along the X-capacitors first, *path 3*, circulates through top and bottom switching positions, *paths 4, 5 and 6*, and finally back to -DC busbar, *paths 7 and 8*.

In module design A, the current circulates through the switches before reaching to the X-capacitors. But as mentioned before, module design B is more preferrable because the current flows through the X-capacitor bank first before reaching to the switches. This helps with better current distribution among the paralleled die and effectiveness of X-capacitors for mitigating voltage transients.

ANSYS Simplorer can bridge between the mechanical design and electrical performance verification. To analyze the current distribution inside the module and especially through each paralleled die on the POL, the whole module net is simulated using ANSYS Simplorer. Figure 3 shows the structure of the simulation. Both modules are full-bridge with symmetrical legs with respect to the busbars, hence, to reduce the simulation time one of the full-bridge legs is kept open-circuited. The other leg is tested in a double pulse test (DPT) mode with the top switch open and bottom switch pulsed.

The current distribution of the four parallel die on the bottom POL is shown in Figures 4(a) and (b). As it can be seen in these figures, the current symmetry of the parallel die is significantly related to the location of the busbars and X-capacitors. And design A does not meet the criteria of symmetrical current distribution across paralleled die.

Although the proximity of the X-capacitors to the switching leg will reduce the loop inductance and overall parasitic voltage overshoot, a smaller loop inductance does not necessarily guarantee the correct operation of the power module. The current circulating from the busbars should flow through the X-capacitors first and then to the switching leg. With wide copper trace design on the switches, the X-capacitors help with the symmetrical distribution of the current along the paralleled die which is critical in fast switching devices such as GaNs.

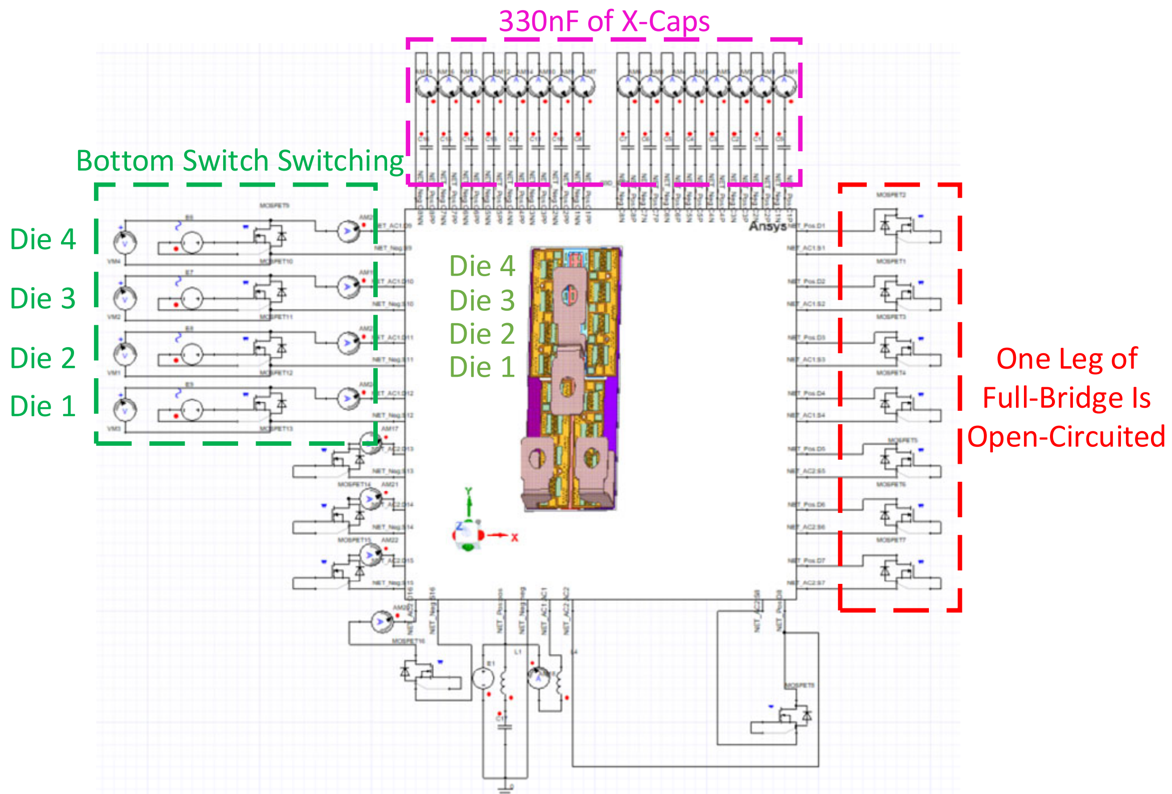



**Figure 3:** ANSYS Simplorer modeling of the designed GaN modules.

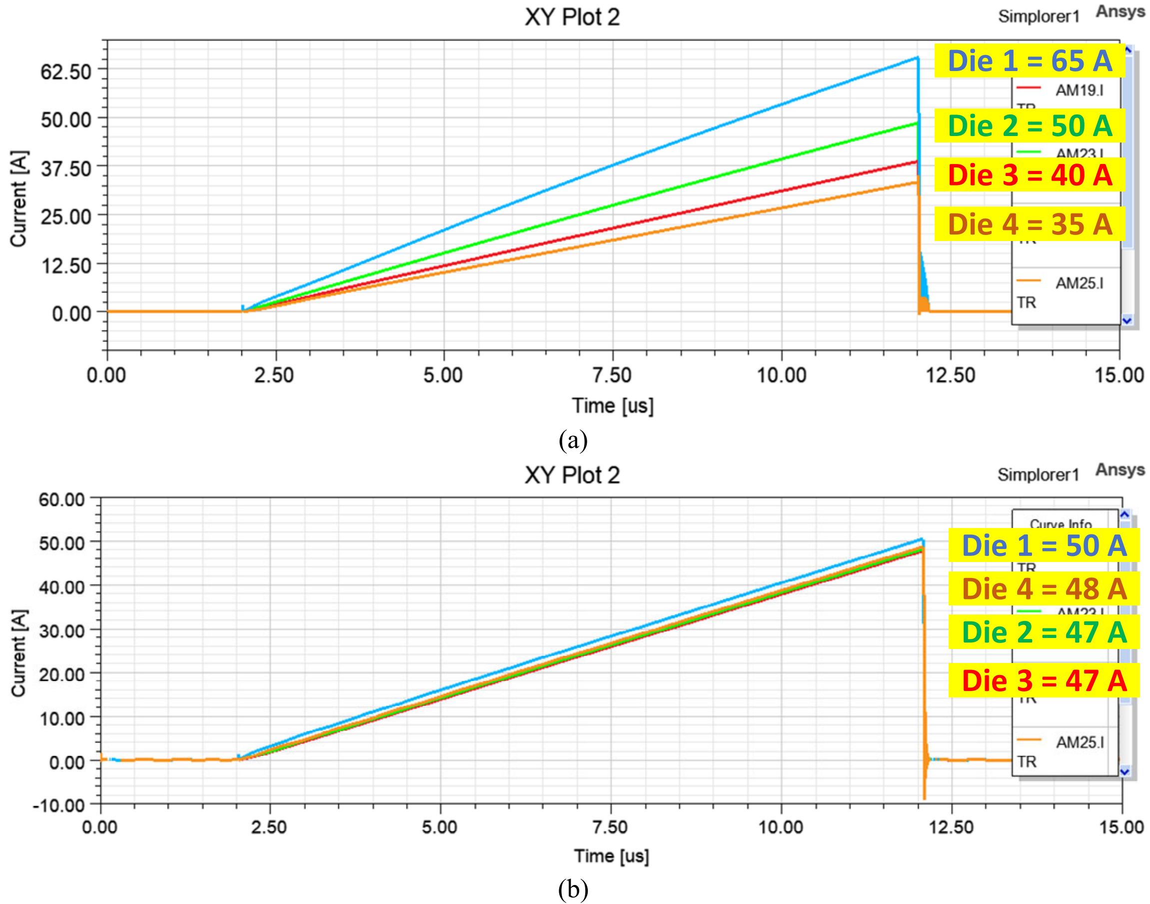



**Figure 4:** Current distribution analysis between four paralleled die on bottom switching position.

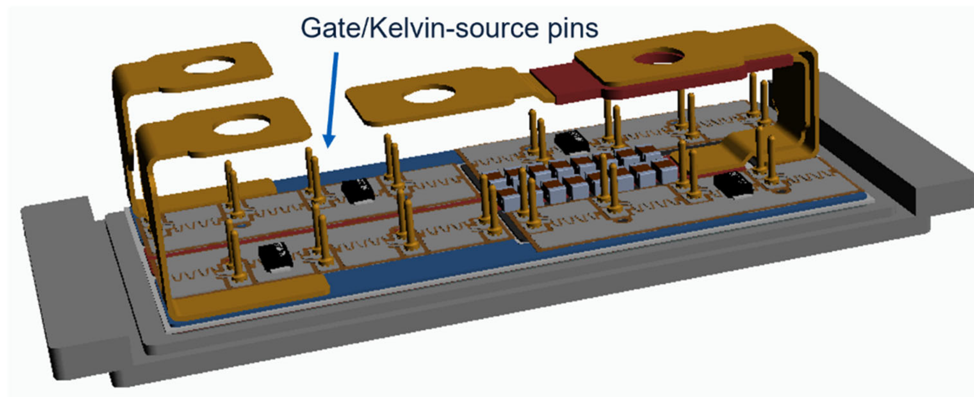
### 3.2. Module Design B: Parasitic Analysis

According to the current distribution results, module design B is selected as the final design for further analyses and fabrication. Parasitic analysis on ANSYS Q3D shows 6nH loop inductance inside the half-bridge switching position to the integrated X-capacitors.

## 4. INTEGRATED GATE DRIVER

Because of fast-switching characteristics of the GaN die, it is critical for all paralleled die in one switching position to turn on simultaneously. For this purpose, the gate driver board is integrated inside the power module with direct pins to each die gate/Kelvin-source pads instead of having single gate/Kelvin-source for all paralleled die. Another important consideration is the length of the traces of gate/Kelvin-source signals on the gate driver PCB. It is more preferrable for the traces to have similar length than for some to be shorter length because the simultaneous turn-on of the paralleled bare die takes precedence to their faster turn-on because GaN devices inherit very fast switching speeds regardless.

As shown in Figure 5(a) and (b), the gate driver board is integrated inside the power module, controlling each paralleled die directly through separate Gate/Kelvin-source pins. The configuration for gate resistor is 20 Ohms total for each gate-source path of GaN die, and the gate driver board has +6V/-4V bias supply. The gate driver was tested with a 560pF capacitor load on gate-source to check the PWM signal and gate-source voltages. Figure 6(a) and (b) show that the propagation delay is about 60nsec for both turn-on and turn-off conditions.

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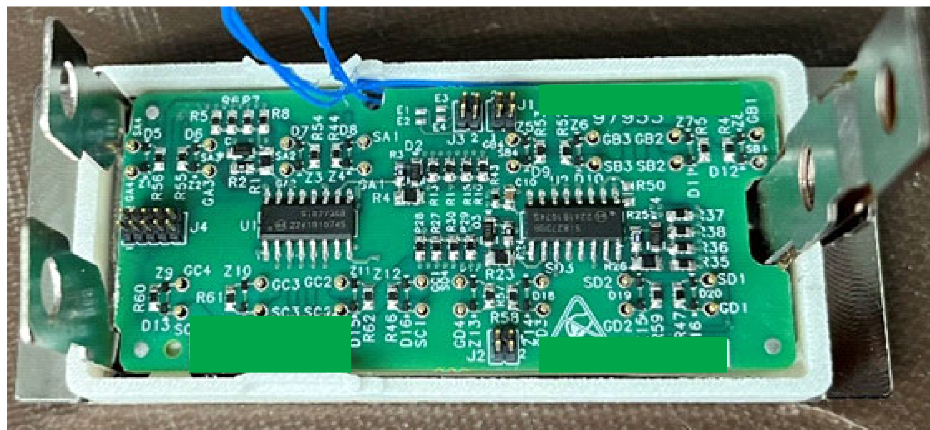
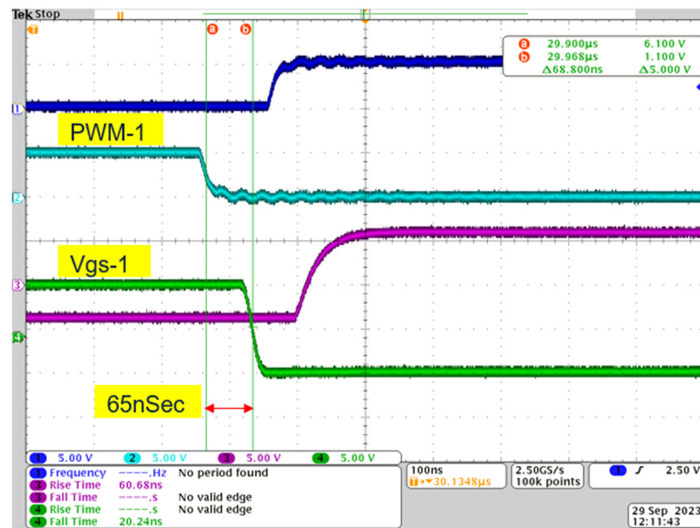


(b)

**Figure 5:** Full-bridge power module, a) separate gate/Kelvin-source pins for paralleled die, b) integrated gate driver.

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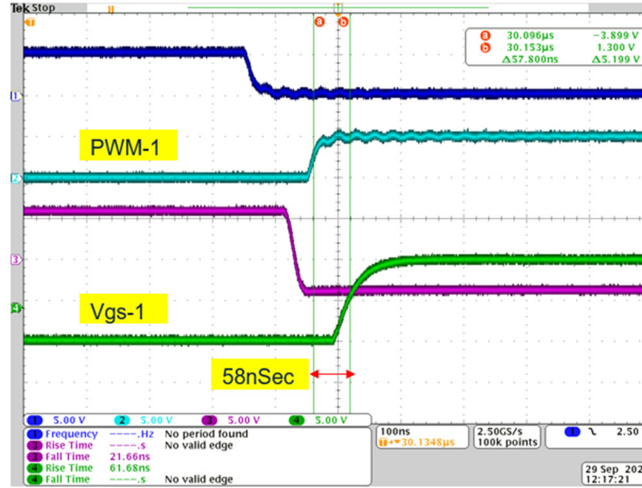



(b)

**Figure 6:** Gate driver propagation delay, a) turn-off, b) turn-on.

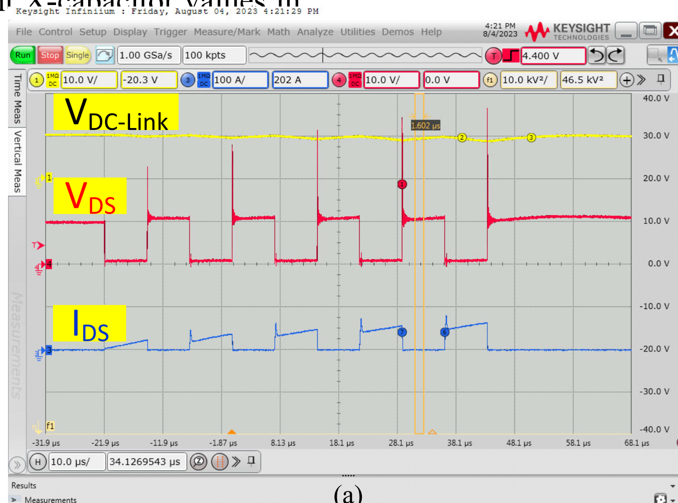
## 5. DOUBLE PULSE TEST (DPT)

### 5.1. Resonance

The advantage of using GaN devices is their capability of fast turn-on and turn-off which reduces the switching losses significantly. Such high di/dt creates high voltage overshoots and prevents the module from getting to its full voltage/current rating without any damage to the devices. Hence, using integrated X-capacitors to minimize the switching loop inductance is crucial especially for GaN modules. While integrated X-capacitors reduce the overall voltage overshoot, they can easily resonate with the busbar inductance and output dc-link capacitor bank. In this section, this resonance is studied for different X-capacitor values in a double-pulse test (DPT) condition. Instead of two pulses, a 100kHz array of pulses is applied to understand the resonance condition in a real switching behavior.

Figure 7(a) is a good representative of using GaN module without integrating X-capacitors. As it can be seen from this test result, the applied current to the module is less than the rated current because the high voltage overshoot does not allow increasing the current any further without passing the voltage limit of the die during overshoot.

The resonance on the switch voltages is shown for a condition with two X-capacitors, eight X-capacitors and sixteen X-capacitors embedded inside three different modules of the same design.

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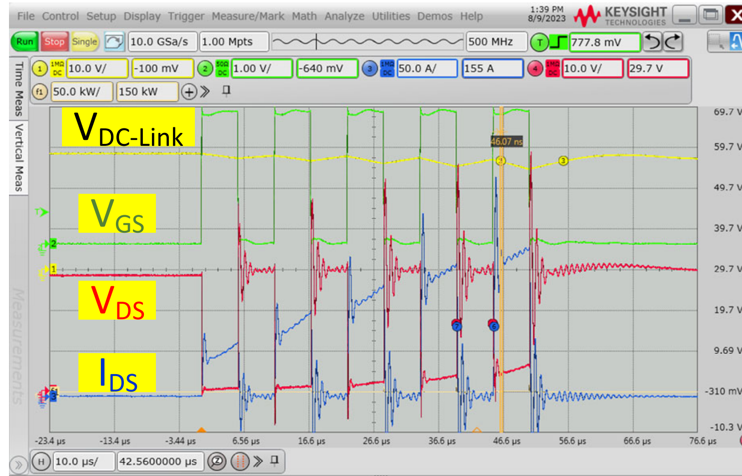

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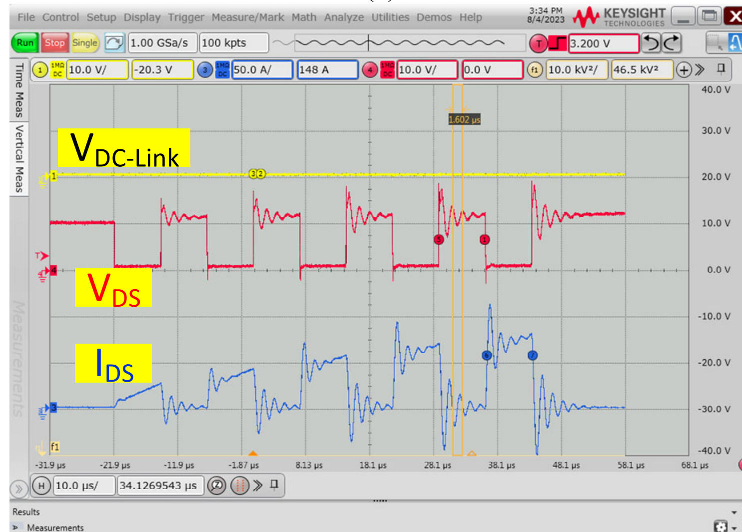

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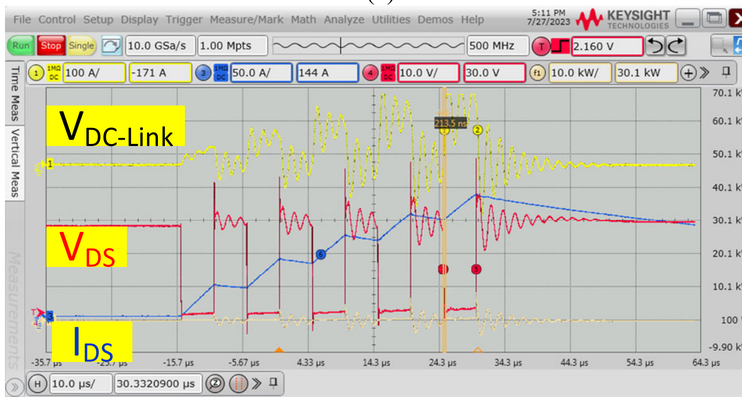


(d)

**Figure 7:** DPT drain-source voltage and current with, a) no X-capacitors, b) two X-capacitors, c) eight X-capacitors, d) sixteen X-capacitors.

As shown in the test results above, the condition with two X-capacitors has a damping resonance in 100kHz switching frequency. There is a resonance of 1MHz on the drain-source voltage of the module with two X-capacitors in parallel. The resonance

frequency is almost similar for both eight and sixteen X-capacitor modules, 660kHz. LTSpice modeling based on ANSYS Q3D parasitic extraction shows the resonance happens among the X-capacitors, dc-link capacitors, and inductance between them.

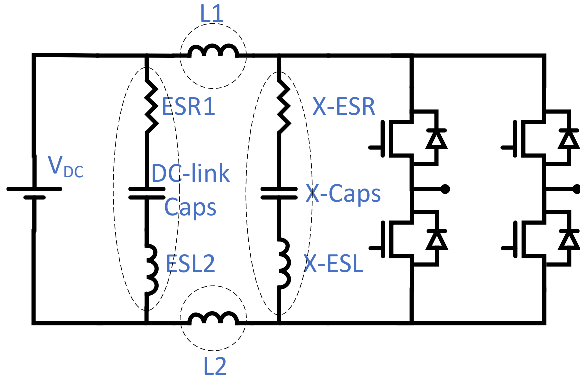



**Figure 8:** Resonating loop in full-bridge module.

Using LTSpice simulations, the losses on two paralleled X-capacitors are significantly high, 3W average losses per capacitor with an ESR of 60$m\Omega$ per capacitor because of the current rating of the module and coolant temperature. This means in a hard-switching condition such as DPT, there should be a compromise between the accepted resonance frequency and the number of X-capacitors in parallel with the switching leg. To understand the effects of such resonance in a system and the importance of reducing the resonance with fewer X-capacitors versus temperature rise on the X-capacitors, the eight, and sixteen X-capacitor modules are being used inside a developmental, isolated DC-DC converter with soft switching. Figure 9 shows the $V_{DS}$ across switches of the two modules in soft switching condition. As shown in Figure 9, in a system-level operation with soft switching the resonance damps easily within the 100kHz switching frequency. Comparing the two drain-source voltages, the module configuration with sixteen X-capacitors is preferrable as the current passing through the X-capacitors will be halved, avoiding any excessive temperature rise on the embedded X-capacitors.

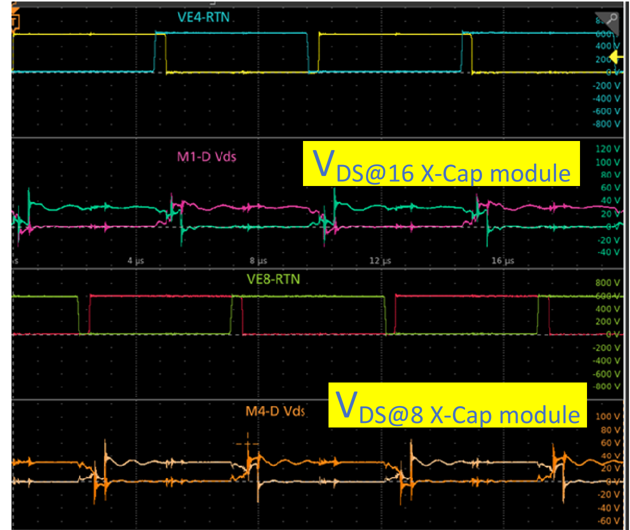



**Figure 9:** $V_{DS}$ of two modules with eight X-capacitors and sixteen X-capacitors in a soft-switching condition.

### 5.2. Switching and $R_{DSon}$ Losses

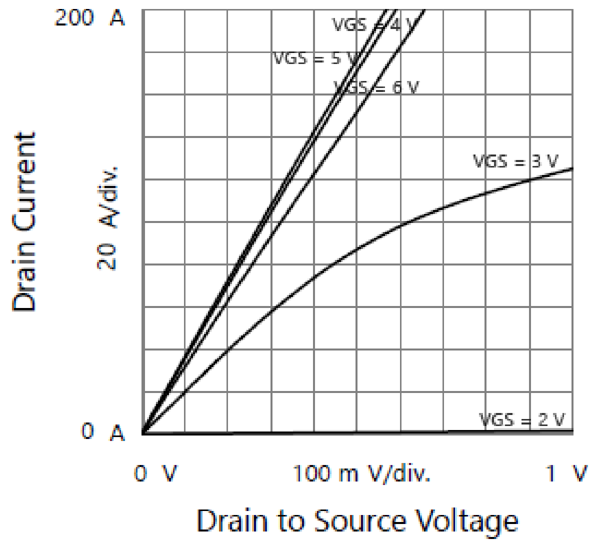
To ensure the module design meets total loss and thermal requirements, static and dynamic tests have been performed to measure the conduction and switching losses, respectively.

*A) GaN Module Static Test*

The static characterization can involve a variety of tests, and in this instance, it covers on-state resistance, output characteristics, transfer characteristics, threshold voltage, and device capacitances. Additionally, high-temperature results will be incorporated, especially focusing on the on-state resistance, which depends significantly on the baseplate temperature in the application. Figures 10(a) and (b) show the GaN module static characteristic measured by a B1506AH71 Power Device Analyzer from Keysight.

Figure 10(a) is obtained by sweeping the drain-source voltage of the module from 0 to 1V and observing the resultant drain current and repeating that with different steps of gate-source voltages to understand the response of the current due to changes in drain-source voltages. This plot can also be used to obtain the on-state resistance, $R_{DSon}$, while sweeping drain-source current as shown in Figure 10(b). It shows the $R_{DSon}$

value of 2.92mΩ for 150A of drain-source current at $V_{gs}$ = 6V at 22˚C lab temperature.

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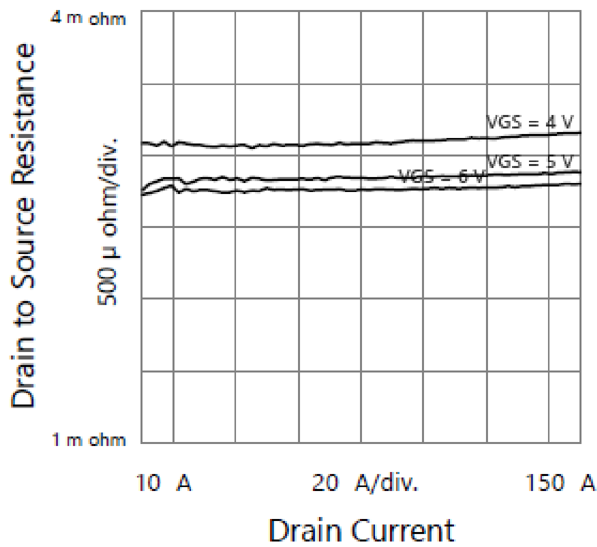



(b)

**Figure 10:** GaN module static characteristics a) output characteristics, b) drain-to-source resistance vs. drain current.

The module is mounted on a cold plate with adjustable coolant temperature. A continuous DC voltage of 6V was applied as $V_{gs}$ for upper and lower switches of right leg and $V_{gs}$ = -4V for both switches on the left leg.

The input current source power supply was adjusted to provide 150A. Figure 11 shows that the $R_{DSon}$ resistance changes from 2.59mΩ to 4.17mΩ across the temperature range, which is a 61% increase, while the GaN die datasheet (GS610008T) shows 75% increase.

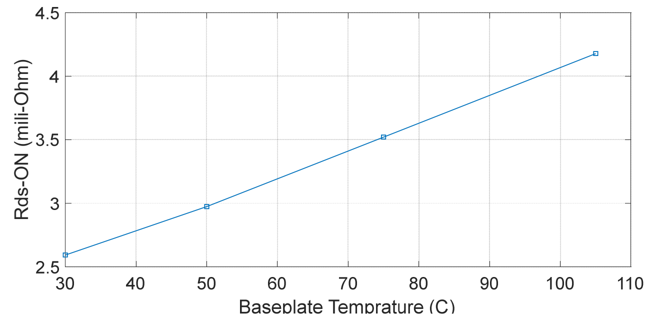



**Figure 11:** $R_{DSon}$ variation vs. temperature.

### B) *GaN Module Dynamic Test*

The hardware DPT setup was assembled to assess the switching losses of the GaN module. The decoupling capacitor board has eleven 10 µF ceramic capacitors, for 110µF total. A film capacitor of 4.5mF is also connected in parallel with the decoupling capacitor board to hold the dc-link voltage. Figure 12(a) shows the single line diagram of DPT including the power train parameters. The integrated gate driver board mentioned in section 4 provides 6V for ON-state and -4V for Off-state. Measuring the switch current directly with X-capacitors embedded inside the power module is not possible. To access the switch current, one Rogowski coil is placed through the negative rail, and one through the lifted X-capacitor, as shown in Figure 12(a). By subtracting the negative-rail current from the total X-capacitor current, the switching current is determined. Figure 12(b) shows the DPT set up partially, which includes GaN module with lifted gate driver board to access the X-Capacitors and decoupling capacitor boards attached to the module DC busbars.

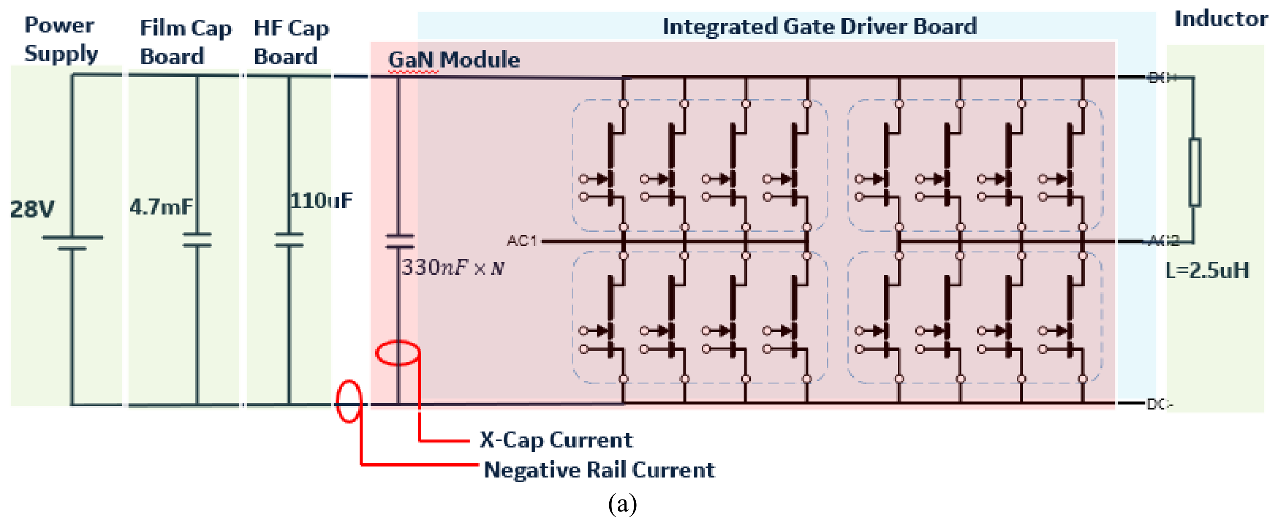
Figure 13 shows the zoomed-in plot of DPT for turn-on and turn-off time intervals. The first pulse was adjusted to drain-source current (Ids), 150A. Upper left gate-source switches received +6V/-4V, labeled Vgs_GB2_SB2 in the waveform, and all other switches had -4V across the gate-source

to avoid any mis-triggering of the lower switches. The switching loss is measured by area under curve of $V_{DS}$ and $I_{DS}$, as illustrated at the bottom of the waveform on Figure 13.

The switching losses and switching speed extracted from oscilloscope waveform is provided in Table 1. The turn-on loss at DPT hard switching is 75µJ, but this can be mitigated by operating in zero-voltage-switching (ZVS) mode. The $V_{DS}$ measurements reached a peak voltage overshoot of 75V at 28V dc-link voltage.

**Table 1:** Switching losses and speeds.

| Transition | Losses (µJ) | Speed (ns) |
|---|---|---|
| **Turn-On** | 75 | 57(Vds-fall_time)<br>39(Ids-rise_time) |
| **Turn-Off** | 8.5 | 11(Vds-rise_time)<br>10(Ids-fall_time) |

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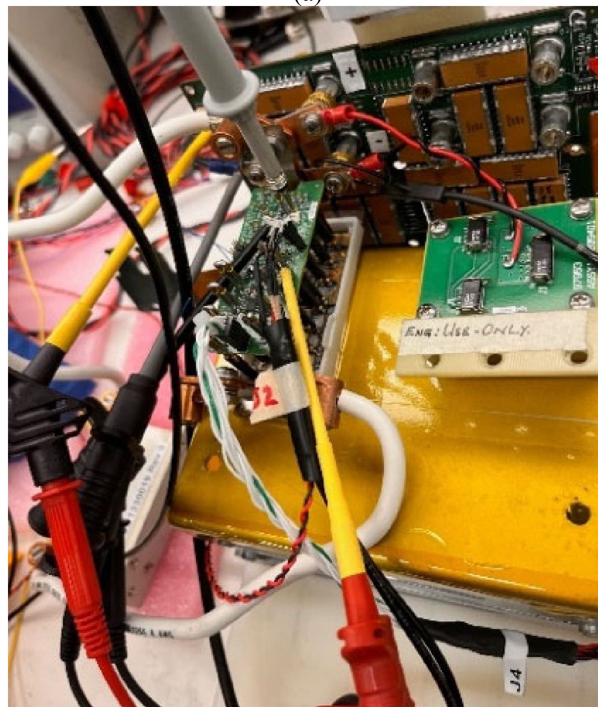

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**Figure 12:** Double Pulse Test (DPT) setup, a) single-line diagram, b) hardware setup.

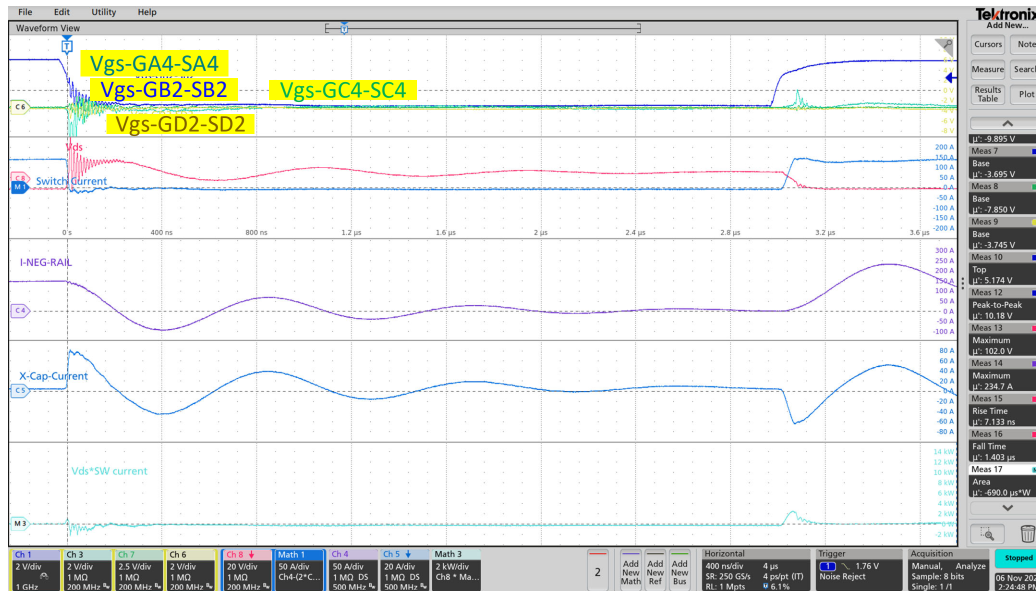


**Figure 13:** DPT waveform for 28V/150A drain-source voltage/current.

## 6. CONCLUSION

Two 100V, 360A full-bridge (FB) GaN module design candidates were studied using ANSYS Q3D and SIMPLORER tools considering current distribution on paralleled die and switching loop inductance. The selected design was fabricated and integrated with embedded switching loop capacitor bank, X-capacitors were added to minimize the loop inductance and reduce the voltage overshoot on the GaN switches in a way that the module could be used with its full current capability. The resonance behavior was analyzed with LTSpice simulation model. Then the resonance behavior with different X-capacitor quantities was studied both in a hard switching condition of a double-pulse test (DPT) and in a soft switching condition of a system-level isolated DC-DC converter. It was shown that the effect of resonance on actual semiconductor devices is not severe in soft switching condition, and it can damp within the switching frequency which allows the use of more X-capacitors in parallel that helps with overall X-capacitor temperature reduction.

The design of the integrated gate driver board to control the paralleled die simultaneously was explained. Moreover, the fabricated module was tested both in static and dynamic conditions to calculate its $R_{DSon}$ and switching losses.

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